PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-329801

(43)Date of publication of application : 30.11.2000

(51)Int.Cl. G01R 21/08
G01R 19/00
G01R 22/00

(21)Application number : 11-142668

(22)Date of filing : 24.05.1999

(71)Applicant : OSAKI ELECTRIC CO LTD

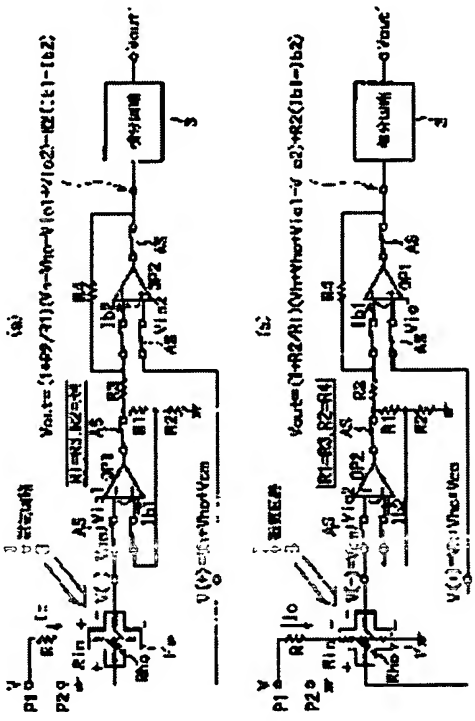
(72)Inventor : KUDO MASAO

(54) SIGNAL DETECTION DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To select and use two operational amplifiers without a condition by removing offset voltages of the two operational amplifiers used in a differential amplifying circuit.

SOLUTION: This signal detection device includes a differential amplifying circuit for the differential amplification of a signal applied between two signal input terminals V(+) and V(-), and an integration circuit 3 for integrating the output of the differential amplifying circuit. The differential amplifying circuit is constructed by connecting an output side of a first operational amplifier OP1 connected to one of the signal input terminals V (+) and V(-), to an inverting input side of a second operational amplifier OP2 connected to the other of the signal input terminals V(+) and V(-). Positions of the first and the second operational amplifiers OP1, OP2 are transposed at half-period intervals of a predetermined signal so that offset voltages thereof cancel each other out in the integration circuit 3.



LEGAL STATUS

[Date of request for examination] 21.08.2001

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the

examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3361480
[Date of registration]	18.10.2002
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention] This invention relates to amelioration of the signal detection equipment which detects the output voltage of a hall device, other voltage signals, etc.
[Description of the Prior Art] In the watthour meter, the hall device is used as one means to measure power (measurement electrical-potential-difference Vx measurement current I). If the field B which is equivalent to the measurement current I on the front face of a sink and a hall device 1 in the hole current Ic equivalent to the measurement electrical potential difference V is given to the input terminal of a hall device 1 as shown in drawing 7 , Hall voltage Vh outputted from a hall device 1 serves as (KxBxIc), and can measure a power value from this Hall voltage Vh. Product sensitivity K is a constant which a hall device 1 has. However, an unnecessary common mode voltage Vcm and offset voltage Vho are contained in power measurement from a hall device 1 at an output. A common mode voltage Vcm hangs the one half of the input resistance Rin of a hall device 1 on the hole current Ic, and is contained in the output terminal (V+) of a hall device 1, and an output terminal (V-). Offset voltage Vho hangs the unbalance resistance Rho on the hole current Ic, and generates it between output terminals (V+) (V-) like Hall voltage Vh. In addition, P1 and P2 are volt input terminals with which the measurement electrical potential difference V is impressed. When measuring electric energy using a hall device 1, in order to remove offset voltage Vho in the latter part, as an amplifying circuit of Hall voltage Vh, the integrating circuit 3 for integrating a power value to electric energy is used using the differential amplifying circuit 2 (amplification factor A) for removing a common mode voltage Vcm. Since offset voltage Vho is the alternating voltage of the same frequency as the measurement electrical potential difference V, by finding the integral, positive/negative is offset and it serves as zero. Consequently, Hall voltage Vh which is equivalent to electric energy with output voltage Vout' of the integrating circuit 3 shown in the following (1) type is detectable.
Vout'=integral (AxVh) .... (1)
Although there are some classes of differential amplifying circuit used as an amplifying circuit of a hall device output, as shown in drawing 8 , in order to suppress the effect of the output resistance of a hall device 1 in the case of the differential amplifying circuit by one operational amplifier (operational amplifier) OP, input resistance R1 of an operational amplifier OP is made larger than the output resistance of a hall device, and in order to obtain an amplification factor A further, it is necessary to make a feedback resister R2 larger than input resistance R1. moreover, output voltage Vout of the operational amplifier OP (differential amplifying circuit) shown in the following (2) types **** -- it is superimposed on the offset voltage Vos of the sum total which consists of offset voltage Vib by the input offset voltage Vio of an operational amplifier OP, input-bias-current Ib+, and Ib- in addition to Hall voltage Vh and offset voltage Vho.
Vout =(R2/R1) (Vh+Vho)+Vos .... (2)
Therefore, output voltage Vout' of an integrating circuit 3 becomes integral {(R2/R1) Vh+Vos}.
[Problem(s) to be Solved by the Invention] Since Hall voltage Vh turns into a minute electrical potential difference in case a light load is measured as a watthour meter, the effect of offset voltage Vos is large, and causes an error. therefore, high -- in order for the input terminal of an impedance operational amplifier to receive, there is also the approach of constituting a differential amplifying circuit with three operational amplifiers, but when the number of operational amplifiers increases, since the effect of the part offset voltage also becomes large, it is desirable to use the differential amplifying circuit by two necessary minimum operational amplifiers, as shown in drawing 9 . in this case, high -- since the input terminal of the impedance operational amplifiers OP1 and OP2 can receive, the effect of the output resistance of a hall device 1 is

suppressed. Moreover, it is good to use the dual operational amplifier which was made on the same pellet and guaranteed the tracking property as a drift decreasing method of the offset voltage of an operational amplifier. However, this approach for which it depends on selection of an operational amplifier as a response to offset voltage Even if it is the drift decreasing method to the last and uses the dual operational amplifier which guaranteed the tracking property The input offset voltage Vio1 of two operational amplifiers OP1 and OP2, and Vio2 Since input bias current Ib1 and Ib2 does not serve as the equivalent thoroughly, the offset voltage by operational amplifiers OP1 and OP2 will remain, as shown in the following (3) types.

Vout =(1+R2/R1)(Vh+Vho-Vio1 +Vio2)

- R2 (Ib1-Ib2) .... (3)

Therefore, output voltage Vout' of an integrating circuit 3 becomes integral {(1+R2/R1) (Vh-Vio1+Vio2) -R2 (Ib1-Ib2)}. Moreover, the operational amplifiers OP1 and OP2 to be used will be made on the same pellet, will have the conditions of the dual operational amplifier which guaranteed the tracking property, and can be applied to an operational amplifier at large.

(The object of invention) The object of this invention is being able to remove the offset voltage of two operational amplifiers used for a differential amplifying circuit, and offering the signal detection equipment which can carry out the selection activity of this two operational amplifier without conditions moreover.

[Means for Solving the Problem] In the signal detection equipment which has the differential amplifying circuit which carries out the differential amplifier of the signal with which this invention is impressed between two signal input terminals in order to attain the above-mentioned object, and the integrating circuit which integrates with the output of this differential amplifying circuit While constituting by connecting the output side of the 1st operational amplifier connected to the reversal input side of the 2nd operational amplifier by which said differential amplifying circuit is connected to one side of said signal input terminal on another side of said signal input terminal It is characterized by replacing the location of said 1st operational amplifier and 2nd operational amplifier for every half period of a predetermined signal with which the offset voltage of said 1st and 2nd operational amplifiers is offset in said integrating circuit.

[Embodiment of the Invention] Drawing 1 is drawing showing the configuration of the important section of the watthour meter using a hall device which is one gestalt of operation of this invention. In drawing 1 , a hall device 1 and an integrating circuit 3 are completely the same as that of what was explained by drawing 7 -9. It considers as the differential amplifying circuit which carries out the differential amplifier of Hall voltage Vh which a hall device 1 outputs, and the operational amplifiers OP1 and OP2 of two noninverting magnification forms are used like what was explained by drawing 9 . The noninverting input edge of an operational amplifier OP2 is connected to one output terminal [of a hall device 1] V (+), and (one signal input terminal of = differential amplifying circuit), the noninverting input edge of an operational amplifier OP1 is connected to the output terminal (signal input terminal of another side of = differential amplifying circuit) of another side of a hall device 1, and the output side of an operational amplifier OP1 is connected to the reversal input side of an operational amplifier OP2. And the location of operational amplifiers OP1 and OP2 is replaced like drawing 1 (a) and drawing 1 (b) for every half period of the measurement electrical potential difference V by the analog switch AS formed in the input side and output side of operational amplifiers OP1 and OP2, respectively. Output voltage Vout of the differential amplifying circuit shown in drawing 9 (3) types - (Vh+Vho-Vio(1+R2/R1) 1+Vio2) It is R2 (Ib1-Ib2). Input off SENTTO electrical potential difference Vio1 of the operational amplifier OP1 of the preceding paragraph Minus and input off SENTTO electrical potential difference Vio2 of the latter operational amplifier OP2 It is added and forward negative polarity appears reversely in Ib1 and Ib2 about input bias current similarly. Therefore, when the location of two operational amplifiers OP1 and OP2 is replaced for every half period of the measurement electrical potential difference V with an analog switch AS, and the condition of drawing 1 (a) and drawing 1 (b) is repeated, and it sees one period of the measurement electrical potential difference V, they are each input offset voltage Vio1 and Vio2. If input bias current Ib1 and Ib2 can be distributed to positive/negative for every half period and it lets an integrating circuit 3 pass, it will be removed. Output voltage Vout of the differential amplifying circuit at this time It is shown by (4) types and (5) types, and output voltage Vout' of an integrating circuit 3 is shown by (6) types. In addition, it is R1=R3 and R2=R4.

Vout =(1+R2/R1)(Vh+Vho-Vio1 +Vio2)

- R2 (Ib1-Ib2) .... (4)

Vout =(1+R2/R1)(Vh+Vho+Vio1 -Vio2)

+ R2 (Ib1-Ib2) .... (5)

Vout'=integral {(1+R2/R1) Vh} .... (6)
The concrete circuit of an analog switch AS is as being shown in drawing 2 . While connection between output terminal [of a hall device 1] V (+) and one noninverting input edge of the operational amplifiers OP1 and OP2 is switched by the analog switch AS 1, output terminal [of a hall device 1] V (-), any of operational amplifiers OP1 and OP2, or connection with the noninverting input edge of another side is switched. While connection between one outgoing end of the operational amplifiers OP1 and OP2 and an integrating circuit 3 is switched by the analog switch AS 2, the connection between one reversal input edge of the operational amplifiers OP1 and OP2 and the node of resistance R3 and R4 is switched. an analog switch AS 3 -- either of the operational amplifiers OP1 and OP2 -- while the connection between the outgoing end of another side and the node of resistance R1 and R3 is switched -- either of the operational amplifiers OP1 and OP2 -- the connection between the reversal input edge of another side and the node of resistance R1 and R2 is switched. Since it is necessary to synchronize the clock CK for controlling analog switches AS1-AS3 with offset voltage Vho, a zero cross signal may be detected using a comparator OP3 from the measurement electrical potential difference V of the same frequency as offset voltage Vho, a zero cross signal may be used as a clock CK as it is, and what carried out dividing by the frequency divider may be used as a clock CK. The wave of each part of drawing 1 at the time of using a zero cross signal as a clock CK as it was is shown in drawing 3 . Since the clock CK reversed in order to control analog switches AS1-AS3 is needed, Inverter IV and Buffer BU are arranged in a comparator OP3 or the frequency divider latter part. Zener diodes ZD1 and ZD2 are connected with a hall device 1 for protection of a comparator OP3. Actuation is explained referring to the wave of each part of drawing 3 . If the field B which is equivalent to the measurement current I on the front face of a sink and a hall device 1 in the hole current Ic equivalent to the measurement electrical potential difference V is given to the input terminal of a hall device 1, Hall voltage Vh outputted from a hall device 1 serves as (KxBxIc), and can measure a power value from this Hall voltage Vh. Product sensitivity K is a constant which a hall device 1 has. However, an unnecessary common mode voltage Vcm and offset voltage Vho are contained in power measurement from a hall device 1 at an output, and these are the things of the same frequency as the measurement electrical potential difference V. A common mode voltage Vcm hangs the one half of the input resistance Rin of a hall device 1 on the hole current Ic, and is contained in the output terminal (V+) of a hall device 1, and an output terminal (V-). For this reason, it is removed by carrying out a differential amplifier. Offset voltage Vho hangs the unbalance resistance Rho on the hole current Ic, and generates it between output terminals (V+) (V-) like Hall voltage Vh. Since offset voltage Vho is the AC signal of the same frequency as the measurement electrical potential difference V, when one period to which the area of positive/negative becomes equal is completed, it is removed in an integrating circuit 3. Similarly, they are the input offset voltage Vio1 of operational amplifiers OP1 and OP2, and Vio2. The offset voltage Vos1 of the sum total which consists of offset voltage by input bias current Ib1 and Ib2, and Vos2 Even if it attaches Offset voltage Vos1 The value of {-(1+R2/R1) Vio1-R2xIb1}, and the value of {(1+R2/R1) Vio1+R2xIb1} for every half period for alternation Offset voltage Vos2 Since the value of {(1+R2/R1) Vio2+R2xIb2} and the value of {-(1+R2/R1) Vio2-R2xIb2} are taken by turns for every half period When one period of the clock CK with which operational amplifiers OP1 and OP2 are replaced is completed, it is removed in an integrating circuit 3. Therefore, as long as the time of the period of the clock CK with which the period and operational amplifiers OP1 and OP2 of offset voltage Vho are replaced synchronizing comes and it is carrying out even the synchronization, the timing which detects electric energy with the output of an integrating circuit 3 (sampling) may be detected for every period, or it may collect in a term what round and it may be detected. Moreover, it may be conditions that a duty ratio is equal, and as long as the clock CK with which operational amplifiers OP1 and OP2 are replaced synchronizes with the timing and offset voltage Vho which detect electric energy (sampling), a frequency may be quick or may be late. However, since it may become that operational amplifiers OP1 and OP2 cannot respond and instability when passing, ** and, it needs to be careful. According to drawing 1 and the operation gestalt of drawing 2 , since the input impedance of the differential amplifying circuit by two operational amplifiers OP1 and OP2 is high, it is not influenced of the output impedance of the hall device 1 used as the sensing section, and also it is not necessary to perform zero adjustment of offset voltage, and can respond also to a drift, and offset voltage can be removed. It does not matter in order to distribute offset voltage to positive/negative also as conditions for the operational amplifier to be used and to cancel, even if offset voltage is larger than a signal level, and is made on the same pellet, and since there are no conditions of the operational amplifier which guaranteed the tracking property, it is applicable to an operational amplifier at large. Drawing 4 is drawing which are other gestalten of operation of

this invention and in which showing the configuration of direct-current potential difference signal detection equipment. When measuring the potential difference of direct current voltage V1 and V2, the differential amplifying circuit and integrating circuit which are shown in drawing 1 are used for this operation gestalt. The noninverting input edge of an operational amplifier OP2 is connected to one signal input terminal of a differential amplifying circuit into which direct current voltage V2 is inputted, the noninverting input edge of an operational amplifier OP1 is connected to the signal input terminal of another side of a differential amplifying circuit into which direct current voltage V1 is inputted, and the output side of an operational amplifier OP1 is connected to the reversal input side of an operational amplifier OP2. And the location of operational amplifiers OP1 and OP2 is replaced like drawing 4 (a) and drawing 4 (b) for every half period of the clock of a predetermined frequency by the analog switch AS formed in the input side and output side of operational amplifiers OP1 and OP2, respectively. The location of two operational amplifiers OP1 and OP2 is replaced for every half period of a clock with an analog switch AS, and they are drawing 4 (a) and drawing 4 . When the condition of (b) is repeated, and it sees one period, they are each input offset voltage Vio1 and Vio2. If input bias current Ib1 and Ib2 can be distributed to positive/negative for every half period and it lets an integrating circuit 3 pass, it will be removed. Output voltage Vout of the differential amplifying circuit at this time When it is shown by (7) types and (8) types and output voltage of an integrating circuit 3 is detected according to this period (sampling), output voltage Vout' of an integrating circuit 3 is shown by (9) types. In addition, it is R1=R3 and R2=R4.

Vout =-(1+R2/R1)(V1-V2+Vio1 -Vio2)
- R2 (Ib1-Ib2) .... (7)

Vout =-(1+R2/R1)(V1-V2-Vio1 +Vio2)
+ R2 (Ib1-Ib2) .... (8)

Vout'=integral {- (1+R2/R1) (V1-V2)} .... (9)

If direct current voltage V1 or V2 is grounded, it is also possible to detect the electrical potential difference to a gland. The concrete circuit of an analog switch AS is as being shown in drawing 5 . Although most is the same as that of drawing 2 , what carried out dividing of the clock from a crystal oscillator 4 in the frequency divider 5 is used as a clock CK which controls analog switches AS1-AS3. If operational amplifiers OP1 and OP2 are replaced with the quick clock CK, dividing will be performed because it may become that operational amplifiers OP1 and OP2 cannot respond and instability. Actuation is explained referring to the wave of each part of drawing 6 . If direct current voltage V1 is impressed to the noninverting input edge of either of the operational amplifiers OP1 and OP2 and direct current voltage V2 is impressed to the noninverting input edge of another side of the operational amplifiers OP1 and OP2, from this differential amplifying circuit, {-(1+R2/R1) (V1-V2)} will be outputted about the potential difference (V1-V2). the offset voltage Vos1 of operational amplifiers OP1 and OP2, and Vos2 ******** -- offset voltage Vos1 The value of {-(1+R2/R1) Vio1-R2xIb1}, and the value of {(1+R2/R1) Vio1+R2xIb1} for every half period of Clock CK for alternation Offset voltage Vos2 Since the value of {(1+R2/R1) Vio2+R2xIb2} and the value of {-(1+R2/R1) Vio2-R2xIb2} are taken by turns for every half period of Clock CK When one period of the clock CK with which operational amplifiers OP1 and OP2 are replaced is completed, it is removed in an integrating circuit 3.

[Effect of the Invention] According to this invention, by the differential amplifying circuit which carries out the differential amplifier of the signal impressed between two signal input terminals, and the integrating circuit which integrates with the output of this differential amplifying circuit, as explained above, when detecting a signal, the offset voltage of two operational amplifiers used for a differential amplifying circuit can be removed, and, moreover, the selection activity of this two operational amplifier can be carried out without conditions.

[Translation done.]

7

【発明の効果】以上説明したように、本発明によれば、２つの信号入力端子の間に印加される信号を差動増幅する差動増幅回路と、該差動増幅回路の出力を積分する積分回路とによって、信号を検出する場合に、差動増幅回路に使用される２個のオペアンプのオフセット電圧を除去することができ、しかも、この２個のオペアンプを条件なしに選択使用することができる。

【図面の簡単な説明】

【図１】本発明の実施の一形態である、ホール素子を用いた電力量計の要部の構成を示す図である。

【図２】図１におけるアナログスイッチの具体的な回路を示す図である。

【図３】図１の各部の波形を示す図である。

【図４】本発明の実施の他の形態である、直流電位差信号検出装置の構成を示す図である。

【図５】図４におけるアナログスイッチの具体的な回路を示す図である。

【図６】図４の各部の波形を示す図である。

【図７】従来のホール素子を用いた電力量計の要部の構成を示す図である。

8

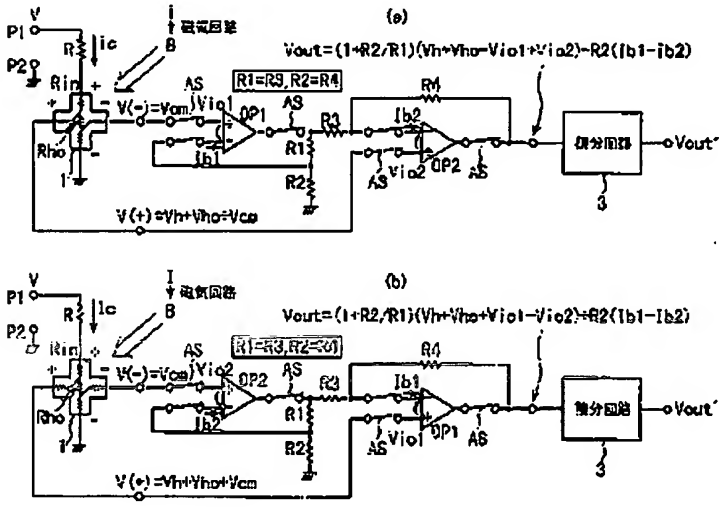
＊【図８】図７における差動増幅回路の一例を示す図である。

【図９】図７における差動増幅回路の他の例を示す図である。

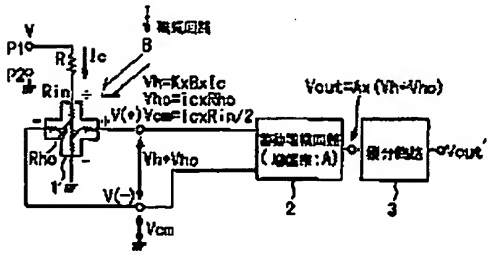
【符号の説明】

１　ホール素子
２　差動増幅回路
３　積分回路
４　水晶発振器
５　分周回路
ＯＰ１，ＯＰ２　オペアンプ
ＡＳ，ＡＳ１，ＡＳ２，ＡＳ３　アナログスイッチ
Ｒ１，Ｒ２，Ｒ３，Ｒ４　抵抗
Ｖ　計測電圧
ｉ　計測電流
Ｖｈ　ホール電圧
Ｖｉｏ１，Ｖｉｏ２　入力オフセット電圧
ｉｂ１，ｉｂ２　入力バイアス電流
Ｖ１，Ｖ２　直流電圧

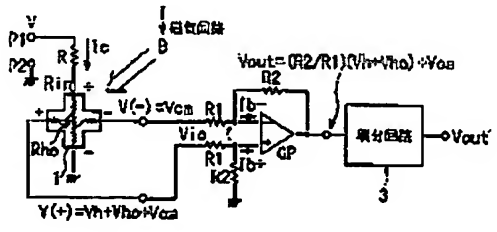
【図１】



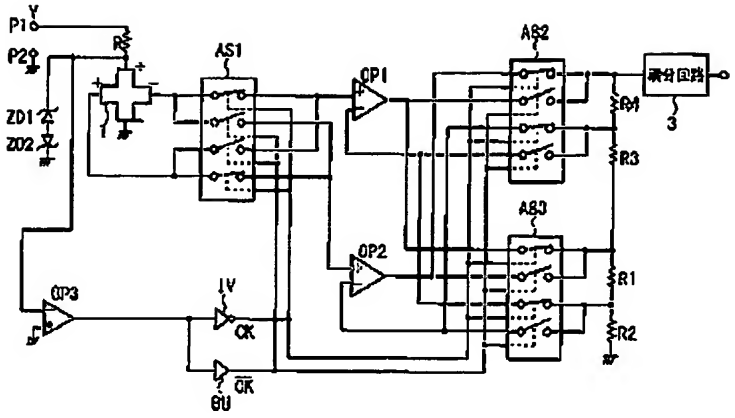
【図７】



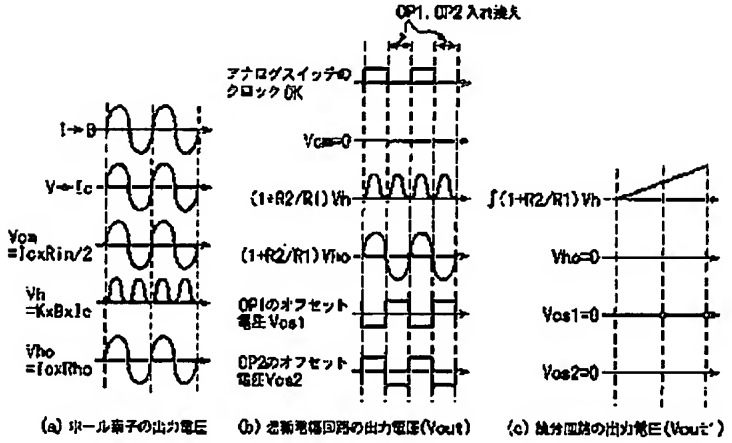
【図８】



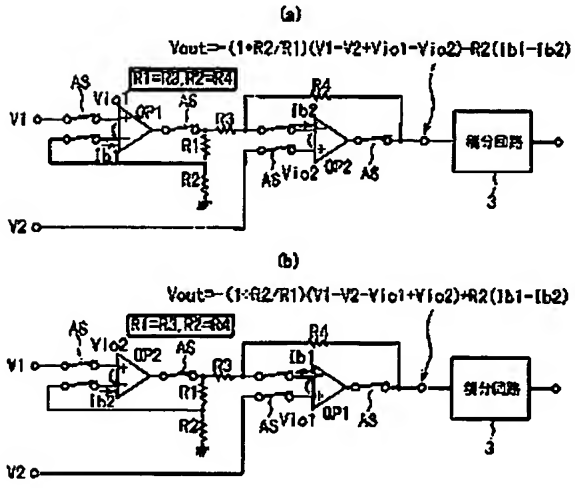
【図2】


P1
P2
R
AS1
OP1
AS2
積分回路
ZD1
ZD2
R4
3
R3
AS3
OP2
R1
OP3
CK
R2
BU

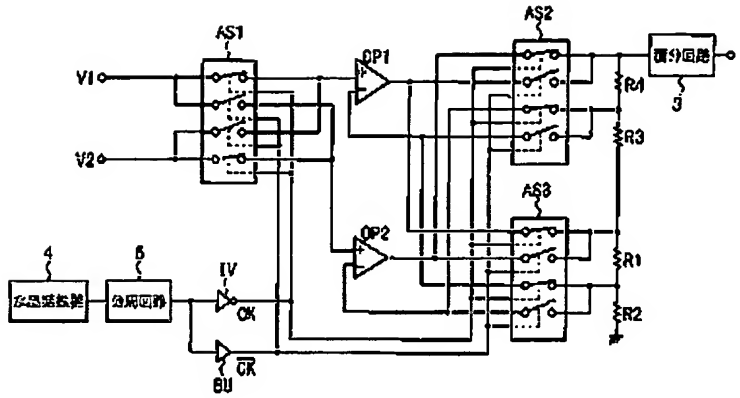
【図3】


OP1, OP2入れ換え
アナログスイッチのクロックCK
I→B
V→Ic
Voa =IcxRin/2
Vh =KxBxIc
Vho =IoxRho
Vcm=0
(1+R2/R1)Vh
(1+R2/R1)Vho
OP1のオフセット電圧Vos1
OP2のオフセット電圧Vos2
∫(1+R2/R1)Vh
Vho=0
Vos1=0
Vos2=0
(a) ホール素子の出力電圧
(b) 差動増幅回路の出力電圧(Vout)
(c) 積分回路の出力電圧(Vout')

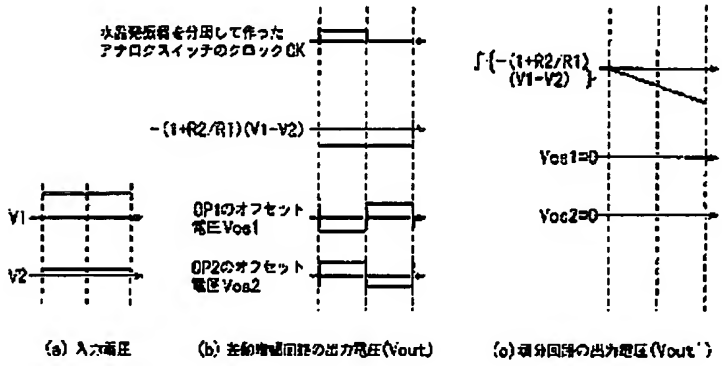
【図4】


(a)
Vout=-(1+R2/R1)(V1-V2+Vio1-Vio2)-R2(Ib1-Ib2)
R1=R3, R2=R4
AS
Vio1
OP1
V1
R4
Ib2
R3
Ib1
R1
R2
Vio2
OP2
積分回路
3
V2
(b)
Vout=-(1+R2/R1)(V1-V2-Vio1+Vio2)+R2(Ib1-Ib2)
R1=R3, R2=R4
Vio2
OP2
Ib1
Vio1
OP1

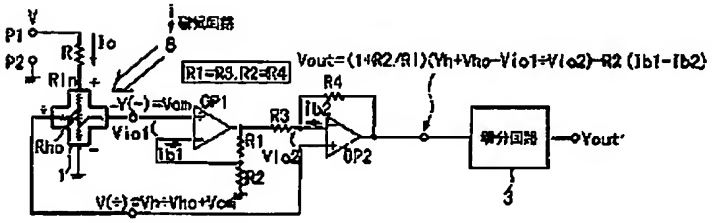
【図5】


AS1
AS2
AS3
OP1
OP2
V1
V2
R4
R3
R1
R2
積分回路
3
4
5
IV
CK
BU
CK

【図6】


水晶発振器を分周して作った
アナログスイッチのクロックCK
-(1+R2/R1)(V1-V2)
V1
V2
OP1のオフセット
電圧Vos1
OP2のオフセット
電圧Vos2
∫{-(1+R2/R1)(V1-V2)}
Vos1=0
Voc2=0
(a) 入力電圧
(b) 差動増幅回路の出力電圧(Vout)
(c) 積分回路の出力電圧(Vout')

【図9】


P1
P2
R
Io
R1
B
R1=R3, R2=R4
Vout=(1+R2/R1)(Vh+Vho-Vio1+Vio2)-R2(Ib1-Ib2)
R4
-V(-)=Vom
OP1
Vio1
Ib1
R3
Ib2
R1
Vio2
OP2
積分回路
Vout'
Rho
R2
V(+)=Vh+Vho+Vos
3